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Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1992. Technical Digest 1992., 14th Annual IEEE
 4-7 Oct. 1992 Page(s):93 - 96
 Digital Object Identifier 10.1109/GAAS.1992.247215
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 Shen-Fu Hsiao; Jen-Yin Chen;
Circuits and Systems, 1997. ISCAS '97., Proceedings of 1997 IEEE International Symposium on
 Volume 3, 9-12 June 1997 Page(s):2068 - 2071 vol.3
 Digital Object Identifier 10.1109/ISCAS.1997.621563
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 Kamp, D.A.; DeVilbiss, A.D.; Haag, G.R.; Russell, K.E.; Derbenwick, G.F.;
Non-Volatile Memory Technology Symposium, 2005
 7-10 Nov. 2005 Page(s):4 pp.
 Digital Object Identifier 10.1109/NVMT.2005.1541393
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- ☐ 4. **ATR's artificial brain ("CAM-Brain") project: A sample of what individual "CoDi-1 Bit" model evolved neural net modules can do with digital and analog I/O**
 de Garis, H.; Buller, A.; Korkin, M.; Gers, F.; Nawa, N.E.; Hough, M.;
Evolvable Hardware, 1999. Proceedings of the First NASA/DoD Workshop on
 19-21 July 1999 Page(s):102 - 110
 Digital Object Identifier 10.1109/EH.1999.785441
[AbstractPlus](#) | Full Text: [PDF\(88 KB\)](#) IEEE CNF
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L6	745355	power near9(rout\$4 or connect\$4 or interconnect\$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/06 12:23
L7	9	L5 and L6 and pad	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/06 12:24
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